

## *Multicore Navigator User Guide*







### **Multicore Navigator User Guide**

KeyStone Architecture Multicore Navigator User's Guide Literature Number: SPRUGR9H November 2010–Revised April 2015

### **KeyStone Architecture Multicore Navigator - Texas Instruments**

KeyStone Architecture Multicore Navigator User's Guide Literature Number: SPRUGR9G November 2010–Revised October 2014

### **KeyStone Architecture Multicore Navigator (Rev. G)**

ø-ii KeyStone Architecture Multicore Navigator User Guide SPRUGR9D+++—January 2012  
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KeyStone Training Multicore Navigator Overview Overview Agenda • What is Navigator? - Definition - Architecture - Queue Manager Sub-System (QMSS) - Packet DMA (PKTDMA) - Descriptors and Queuing • What can Navigator do? ... Multicore Navigator User Guide

### **KeyStone Training Multicore Navigator Overview**

What is Multicore Navigator? • Multicore Navigator is a hardware mechanism that facilitates data movement and multicore co-working • Supports multiple users (players) -Each core in a multicore system -High bit-rate peripherals including SRIO, AIF2, Network Coprocessor (NETCP), and PCIe • Users can think of the Navigator as a mailbox ...

### **Using Multicore Navigator - Texas Instruments**

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### **HORRYGEORGETOWNTECH.ORG Online Library Ebook and Manual ...**

• Multicore Navigator is a collection of hardware components that facilitate data movement and multi-core control. • The major components within the Navigator domain are: -A hardware Queue Manager (QM). -Specialized packet DMAs, called PKTDMA. -Data structures to describe packets, called descriptors.

### **KeyStone Training Multicore Navigator Overview**

Page 2 of 22 Multicore Navigator for Dummies Application Report <SPRA##>—August 2012 Submit Documentation Feedback 1 The History of Multicore Navigator (According to Me) or Why Multicore Navigator www.ti.com 1 The History of Multicore Navigator (According to Me) or Why Multicore Navigator

### **Multicore Navigator for Dummies - Texas Instruments**

Multicore Programming Guide Multicore Programming and Applications/DSP Systems Abstract As application complexity continues to grow, we have reached a limit on increasing performance by merely scaling clock speed. To meet the ever-increasing processing demand, modern System-On-Chip solutions contain multiple processing cores. The

### **Multicore Programming and Applications/DSP Systems**

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### **Telstra User Guide - ibi.illinoisbackpain.com**

It can however be used in a chain so that the output queue can trigger the input channel of a peripheral's pktDMA. The Infrastructure pktDMA has 32 channels, so it can process 32 transfers

simultaneously. You can refer to the Multicore Navigator User Guide on TI.com (search for SPRUGR9E) for more details. -dave

**Multicore Navigator Tips 'n Tricks, pt. 2 - The Process ...**

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